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Typed or printed name MARK L BECKER	2	-0					1
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This collection of information is required by 37 CFR 1.5. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentially is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to 12 minutes to complete, including gathering, preparing, and submitting the completed application form for the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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FEE TRANSMITTAL				Complete if Known						
				Application Number 10/082,050						
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				First Named Inventor Stephe			en R Čebenko			
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Applicant claims small entity status. See 37 CFR 1.27				Art Unit 2818						
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Name (Print/Typs)		Registration No. 31325 Telephone 503-268-8629								
Signature						Date	2/4/2004			

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PAGE 2/11\* RCVD AT 2/4/2004 5:41:13 PM [Eastern Standard Time] \* SVR:USPTO-EFXRF-1/1 \* DNIS:8729306 \* CSID:503 268 8077 \* DURATION (mm-ss):03-16

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## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

FEB 04 2004

OFFICIAL

First Named Inventor: Stephen R. Cebenko

Application No.: 10/082,050

Filed: 02/14/2002

For: INTEGRATED CIRCUIT BASE

TRANSISTOR STRUCTURE AND

ASSOCIATED PROGRAMMABLE CELL

LIBRARY

Examiner: Dao H Nguyen

Art Unit: 2818

Attorney Docket No.: 1-1-3-1-1

## CERTIFICATE OF TRANSMISSION

I hereby certify that this paper and the documents referred to as being attached or enclosed herewith are being filed with the United States Patent and Trademark Office by facsimile transmission to 703-

872-9306 on February + 2004.

Mark L. Becker Attorney for Applicants

## **RESPONSE**

Applicants respond to the Office action mailed 10/23/2003, as follows.

one of the multiplous of the base transistor structures, arranged immediately adjacent on another, is configurable to provide gate isolation for active transistors in other ones of the base transistor structures." The claimed gate isolation is electrical isolation provided by tying the separate gates of an intermediate base transistor structure to VDD and VSS, as explained in the amended paragraph. In contrast, the isolation described in Shaw is the physical isolation of transistors' diffused regions (sources and drains). Col. 29, lines 37-45 and the Abstract.

Shaw further does not disclose the limitations of dependent claims 7-17 or of new claims 21-22.

For the above reasons, applicants submit that the present claims are in condition for allowance, and respectfully request such action.

Please call the undersigned if he can be of any assistance in this case.

By: Wela

Respectfully submitted,

Date: \_\_\_\_\_*Z*//

Mark L. Becker

Associate General Counsel, IP

Reg. No. 31,325

Lattice Semiconductor Corporation 5555 NE Moore Ct. Hillsboro, OR 97124

Phone: 503-268-8629 Fax: 503-268-8459

mark.becker@latticesemi.com